

PCB 76504

28.1 Introduction

The A2 board is interposed between the A1 board and the oscillator output, and carries out the following processes:

- Derives a square wave from the main oscillator input;
- Switches and/or mixes various combinations of main, secondary and derived square wave inputs to produce the required composite output signal for a selected measurement;
- Provides an opto-isolated "sync" output;
- Controls output level control from +30 dbu (balanced) to -70 dbu in 0.1 dB steps;
- Allows front panel level trim of ± 0.1 dB;
- Supplies a balanced output capable of driving +30 dbu source EMF into 300 Ω minimum load, from source impedances of 2 Ω , 150 Ω , and 600 Ω ;
- Provides a balanced or unbalanced output.

The output from the main (low distortion) oscillator normally appears at the output alone, except for the following conditions:

SQUARE WAVE	Square wave alone
I.M.D. (1:1)	$(0.707 \times \text{main osc}) + (0.707 \times \text{second osc})$
I.M.D. (4:1)	$(\text{main osc (low frequency)}) + (0.25 \times \text{second osc})$
D.I.M.-30	$(\text{square wave}) + (0.18 \times \text{second osc})$
D.I.M.-100	$(\text{square wave}) + (0.18 \times \text{second osc})$
WOW and FLUTTER	Second oscillator input only

Other combinations for different standards may also be accommodated with the appropriate software (and possibly hardware) updates.

The front panel level trim control can be disabled under remote control.

Figure 28.1.1 shows the block diagram of the A2 board.

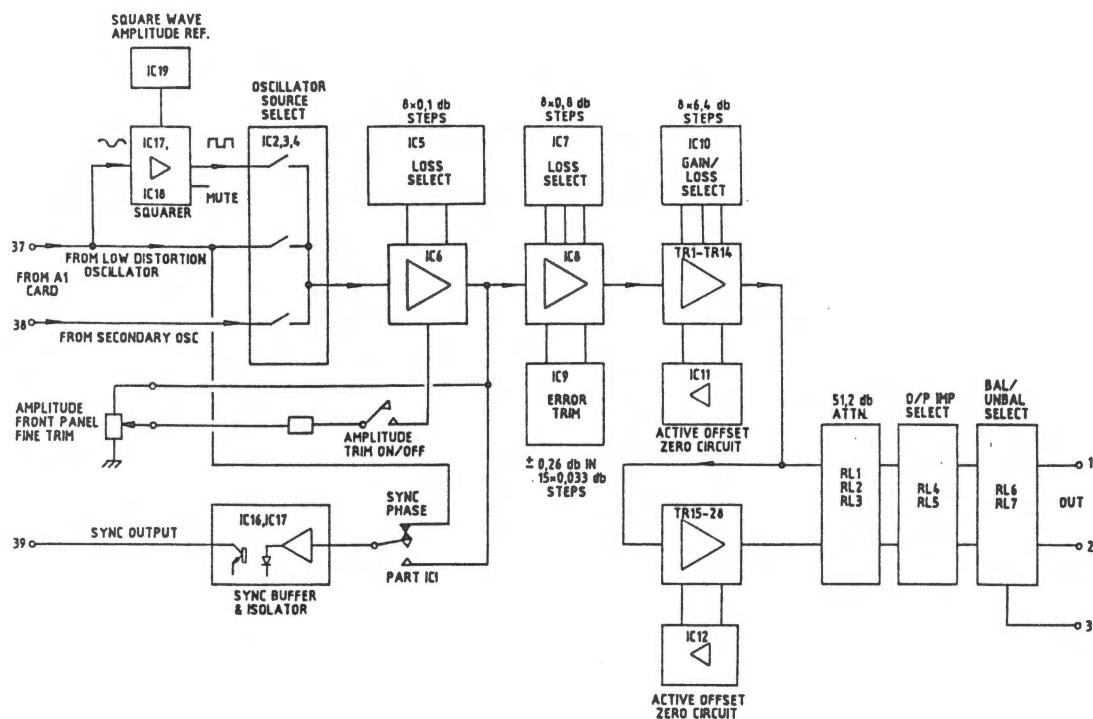


Figure 28.1.1 MD404B Analogue 2 Board - Block Diagram

28.2 Circuit Description

28.2.1 Squarer

The main oscillator input, appearing on pin 37 at a level of 5 V peak, is fed into the non-inverting input of comparator IC18. The other input of IC18 is connected to the ground rail. IC18 output therefore changes state each time the sine wave at the non-inverting input crosses through zero. The square wave output at pin 7 of IC18 changes state between +4 V and +9 V. This square wave is connected to a control input of analogue switch IC1, pin 11. The "normally open" and "normally closed" positions (pins 12 and 13) of IC1 are connected to stable ± 6.1 V voltage sources (the exact voltage is variable to set the level despite component tolerances, but the chosen voltage is stable). A square wave of ± 6.1 V with exact amplitude symmetry about 0 V and unity mark:space ratio appears at IC1 pin 14 (changeover switch common) and is fed to part of the oscillator source select switch circuitry, via RN3A & B, RN4B, RN5B, RN4A and RN5A.

Stable square wave amplitude is provided by a voltage regulator IC19, and a negative version of the reference voltage appears at the output of unity gain inverter IC17. VR1 is used to adjust the square wave amplitude and VR2 the amplitude symmetry.

The comparator is disabled when the square wave is not required, by turning on transistor TR29 from the data latch IC15 pin 16. With +9 V on TR29 base, R63 causes a current of about 3.5 mA to be drawn from IC18 pin 6, forcing IC18 output 7 to a high state.

The preset VR3 is used to adjust the mark:space ratio of the square wave to exactly 1:1, effectively trimming out any offset voltages on the main oscillator signal or IC18 input.

28.2.2 Input Selection Circuit

The analogue switches IC2, IC3 and IC4, select combinations of signals originating from the main and secondary oscillators, plus the output from the square wave circuit. The analogue switch sections either route the signals to the virtual earth input formed at the input of inverting amplifier IC6 or ground. This arrangement minimises breakthrough from unselected signals, as well as minimising distortion due to switch element non-linearity. The switching arrangements of the two oscillator and one square wave source are programmed according to the required output test signal requirements, as set out in the table below:-

MODE	Analogue Switches "Made"
Sine Wave	IC2 Pins 14-13
Square Wave	IC3 Pins 14-13
I.M.D. (1:1)	IC2 Pins 15-1
I.M.D. (4:1)	IC2 Pins 14-13, IC4 Pins 15-1
D.I.M.-30	IC3 Pins 4-3
D.I.M.-100	IC3 Pins 15-1
W & F	IC4 Pins 14-13

Combinations of signals other than those listed above for different test signal requirements can be obtained by making the appropriate link LK1 or LK2, but this can only be done in conjunction with appropriate software.

The low pass filters RN3A and B with C1, RN4B and RN5B with C2, provide the required square wave filtering specified in the D.I.M.-30 and D.I.M.-100 standards, respectively.

The low pass filter network RN4A, RN5A and C3, removes overshoot on the square wave in the "square wave only" output mode. The same purpose is also served by C57, effectively switched in parallel with RN3B, the feedback resistor for IC6.

The control inputs for the analogue switches IC2, IC3 and IC4 are latched across from the isolated data bus by IC17, an octal D-type flip-flop. The analogue switch ICs are powered from +9 V and -9 V rails, while the control logic levels are +9 V and +4 V.

28.2.3 First Amplifier

The input signals from the combination of main/secondary oscillators and/or square wave are mixed together at the inverting input of IC6. The gain of the amplifier stage comprising IC6, feedback resistor RN3B, and input networks and switches, is so arranged as to provide a constant R.M.S. output signal level at IC6 pin 6, regardless of the input signal selected. For a sine wave input (5 V peak at main input or 10 V peak at secondary oscillator input) the signal amplitude will be approximately 8.68 V peak. The gain of this stage can be reduced in 0.1 dB steps by up to 0.7 dB, by a weighted value resistor RN8A, RN8B, and RN8C, effectively switched in parallel with IC6 feedback resistor RN9B by analogue switch IC5 sections. The gain reduction is effected by resistor/switch combinations as set out in the table below:-

Gain Reduction (dB)	Resistors Across RN9B	Analogue Switch Section Made
0	None	None
0.1	RN8A	4-3
0.2	RN8B	15-1
0.3	RN8A, RN8B	4-3, 15-1
0.4	RN9A	14-13
0.5	RN8A, RN9A	4-3, 14-13
0.6	RN8B, RN9A	15-1, 14-13
0.7	RN8A, RN8B, RN9A	4-3, 15-1, 14-13

The switched ends of RN8A, RN8B and RN9A are grounded by the analogue switch sections when not in circuit, in a similar manner to the analogue switch sections within IC2, IC3, and IC4.

28.2.4 Fine Level Control

The front panel level trim control is a potentiometer whose ends are connected between IC6 output and ground. The slider from the trim control is connected to one end of R65, so that R65 is progressively introduced in parallel with IC6 feedback resistor RN9B provided that the analogue switch section in series with R65 (IC2 pins 4-5) is made.

This provides a further maximum gain reduction around IC6 of 0.2 dB, effectively giving a gain trim range of ± 0.1 dB. The level trim control can be switched out of circuit by IC2. In order to make the trim range ± 0.1 dB rather than 0 dB to -0.2 dB, the operating programme switches the gain by 0.1 dB when the fine level control is switched in or out.

28.2.5 Second Amplifier

The signal from the first amplifier is fed to IC8 via IC7, a 1-of-8 analogue multiplexer. IC7 selects one of eight pairs of gain-setting resistors, made up from RN10 to RN14. These gains are from slightly over unity to -5.6 dB in 0.8 dB steps. IC8 functions as an inverting amplifier. C10 and RN11F are to stabilise IC8.

28.2.6 Gain Trim Steps

All the feedback resistors round IC8 are the same value. This makes it possible to switch high value resistors in parallel in order to trim out variations in gain due to resistor tolerance. The trim components used are RN15A to RN15D, which are binary weighted. The overall step size is reduced by R66. The actual step size is approximately 0.033 dB.

The steps are switched in or out by IC9 and one section of IC1, controlled by bits 1 to 4 of IC15, an octal D-type flip-flop.

28.2.7 Output Amplifiers

Figure 28.2.1 shows a simplified circuit of the MD404B output system.

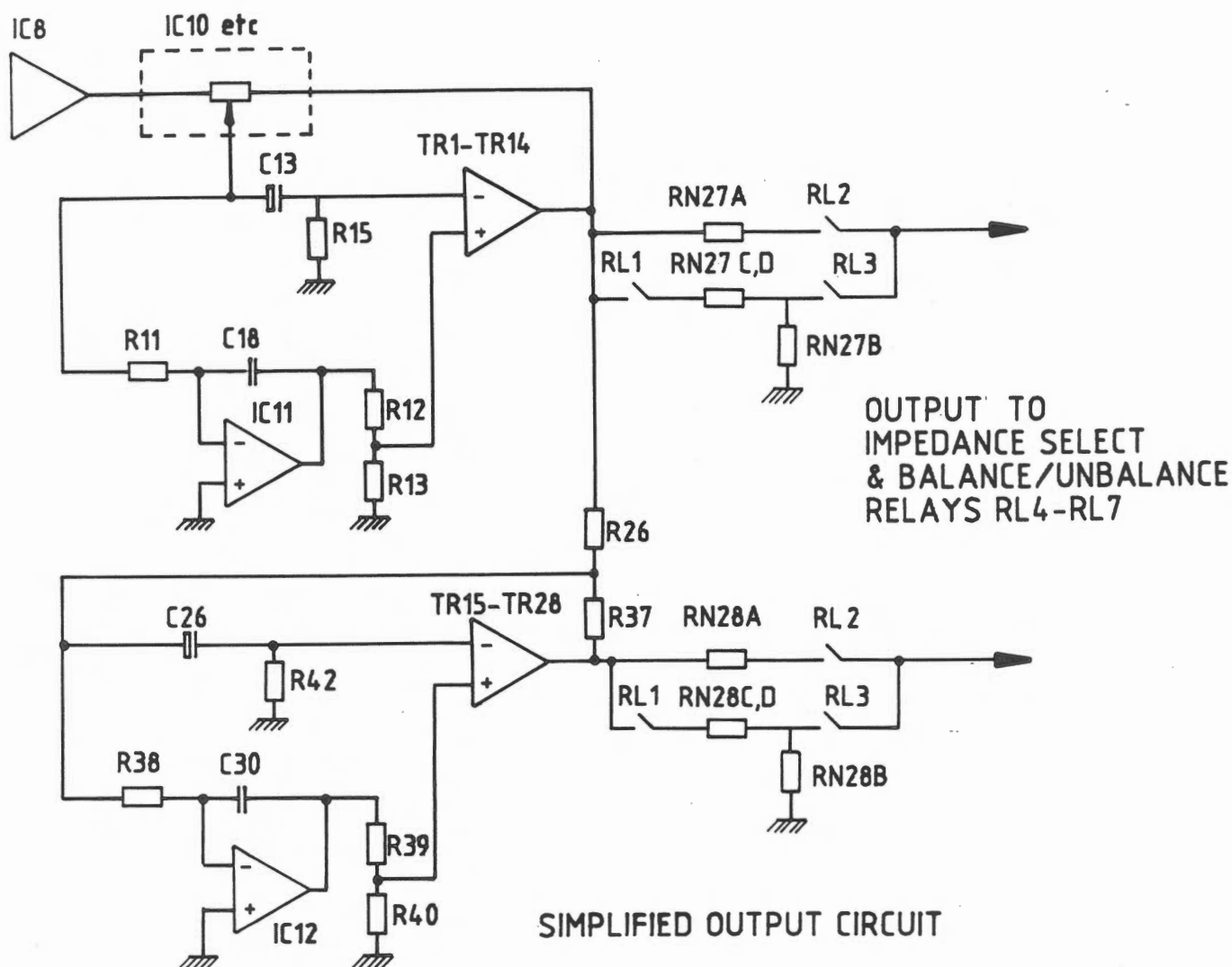


Figure 28.2.1 MD404B Simplified Output Circuit

TR1-TR14 form an op-amp of high voltage, current and power bandwidth capability. TR1 and TR2 are a differential pair, with emitter current supplied by R14. TR1 is the non-inverting input. Its output is fed to TR4, which passes a non-inverted signal on to TR5. TR2's output feeds TR3, which passes an inverted signal on to TR8. TR5 and TR8 provide the majority of the voltage gain of the entire amplifier. TR6 and TR7 are diode connected in order to provide temperature compensated bias to the output stage halves.

TR9 acts as the driver transistor for TR11 and TR12, the output transistors of the top half output stage. R9 and R10 ensure current sharing between TR11 and TR12. D2 and TR6 limit the drive to about 1.2 V across TR9 and R19, and so the maximum voltage which can appear across R19 is about 0.6 V, thus limiting the output stage current to about 130 mA.

TR10, TR13 and TR14 operate similarly as the lower half output stage. Current limiting is again applied by D3 and R21.

The input offset voltage, bias current, etc. of the op-amp thus formed is

poor. IC11, via R11, detects any offset voltage at the summing junction. The voltage is integrated in C18, and a proportion is fed back to the non-inverting input of the output amplifier via R12 and R13. The offset voltage at the summing junction is thus kept to the input offset voltage of IC11, which is very low. Bias for the inverting input (TR2 base) is provided by R15.

R1 and C12 stabilise the output amplifier. D1 prevents saturation of TR5.

TR15-TR28, IC12, etc. form an identical output amplifier. The gain is set to -1 by R26 and R37. In balanced mode, the output presented to the outside world is taken between the outputs of the two amplifiers. In unbalanced mode, only the upper amplifier (TR1-TR12) is connected to the load.

28.2.8 Output Amplifier Gain Control

IC10 is a 1-of-8 analogue multiplexer, connecting one of the eight sets of gain setting resistors RN16 to RN23 around the main output amplifier. The resistors are arranged to give gain control from +6 dB to -38.8 dB in 6.4 dB steps. RN16B and RN20B to RN23B keep the voltage swing of the non-selected gain steps within the voltage rails (± 16 V) of IC10.

IC13 bits 6 and 7, and IC15 bit 0, control IC10.

28.2.9 51.2 dB Gain Step

RN27B, C and D provide 51.2 dB attenuation with an output resistance of 1 Ω . RN27A provides 0 dB attenuation with 1 Ω output resistance. RL2 is switched in for 0 dB attenuation; RL1 and RL3 are switched in for 51.2 dB attenuation. The same output resistance applies whichever attenuation is selected.

When the oscillator is muted, RL3 is made, but RL1 and RL2 are not. Thus the output resistance is maintained at 1 Ω with no noise contribution.

The lower output amplifier has an identical system.

28.2.10 Output Resistance Selection

The signals emerging from the 51.2 dB attenuator stage (either attenuated or direct) appear from a source resistance of 1 Ω per side (2 Ω balanced). If this is the chosen output resistance, RL4 is made, and the signals are transferred directly to the outside world.

RN29 and RN24 build out the output resistance to the middle value (usually 150 Ω), with RL5 made and RL4 open. RN25 and RN26 build out further, to the maximum output resistance (usually 600 Ω), with RL4 and RL5 open.

In unbalanced mode, the higher output resistances are disbarred in software, because the hardware cannot provide the required output resistance.

28.2.11 Sync Circuit

An isolated sync circuit is provided at pin 39 on the board edge connector. The sync signal is either derived from the main (low distortion) oscillator input, or the output of IC6. The source selection for the sync circuit is via RN1A, B, C and D, through IC1 pins 3 or 5 to pin 4. The signal is then routed

to voltage follower IC17, and the buffered signal is taken from IC17 output via C52 and R56. The signal increases or cuts off the current flowing through the opto-coupler IC16 LED on alternate half cycles, thus turning the photo diode/transistor part of IC16 on and off, providing a nearly square wave of approximately equal mark:space ratio, alternating between 0 V and +1 V.

The source select analogue switch section IC1 control pin 9 is driven by pin 19 of data latch IC15.

28.2.12 Sub-Rail Power

The +9 V and +4 V for the analogue switch ICs is derived from the +23 V rail by 5 V regulator IC20, with 3.9 V Zener diode D10 in series with the "common" connection at IC20. Input and output decoupling for IC20 is provided by C60 and C61 respectively.

The -9 V rail for the analogue switch ICs is derived from the -16 V rail via R68, and shunt regulated by 9.1 V Zener diode D9.

28.3 Removal/Replacement

Removal and replacement of the A2 board are dealt with in section 25 of this manual. It is important that these details are closely followed in order to avoid damage to, or malfunctioning of, the MD404B oscillator.

28.3.1 Accessing the A2 Board While Live

After following the removal instructions in section 25 as far as removal of the A2 board, the A2 board can be pushed back onto the pins of the "comb" connector of the digital board the "wrong way up", i.e. with the A2 board above the digital board, and the "comb" pins entering the A2 board connectors from the wrong side. This operation must be performed **very carefully** because it is very easy to fail to mate one (or more) pins of the comb and bend them.

The A1 board may then be added in its normal position (with respect to the digital board). The A2 board may now be accessed from both sides, while all boards are connected up and able to fully work.

Insert one of the long screws into the middle pillar set to strengthen the board set and remove the mechanical stress from the "comb" connector.

28.4 Fault Finding

28.4.1 No Output

Using an oscilloscope, check that an input signal to the A2 board is present on pin 37 of the edge connector (A1 board main oscillator output). There should be a sine wave present with approx 10 V pk-pk amplitude. If not the power supply should be checked, and if correct, the A1 board is faulty - see section 27 - A1 board fault finding.

If the 10 V pk-pk sine wave is present, check the output of IC6 at pin 6 with the oscilloscope. The signal present should again be approx 10 V pk-pk varying by approximately 10 % as the level control is turned. If the signal is absent, check the d.c. voltage at IC2 pin 14; this should be +9 V. If not, the fault is in IC14 or associated components. If +9 V is present, IC2 or connections to it should be suspected.

If the signal is present at IC6 output, check IC8 output (pin 6). If no signal is present, check IC8, IC7, and associated components. If the signal is present at IC8 output, check the signal at either end of L1. If the signal is present there it must be broken somewhere in the impedance switching network. If the signal at L1 appears to be correct, switch the output impedance to "0" and observe the waveform at L1. If it clips and diminishes in amplitude, suspect a short circuit in the output impedance selection circuitry or wiring.

28.4.2 Output Distortion When Feeding Low Loads

Check operation of TR11, 12, 13 and 14, and also TR25, 26, 27 and 28.

28.4.3 D.C. On Output

Check all power supply rail voltages. Measure the offset voltage on IC8; it should be within ± 10 millivolts. If the offset appears to be substantially larger than that, remove IC3. If the d.c. disappears then check IC3 pins 9, 10 and 11. They should all be at +4 V (off). If pins 9, 10 or 11 are high, then suspect one of the square wave on/off control latch sections, i.e. IC14 pins 6, 9 and 12. If the switch control lines are all low, suspect IC3.

The foregoing paragraph checks that the D.C. is not present as the result of the square wave input to IC8 being switched on by a fault condition. Under these circumstances the square wave comparator IC18 is still disabled by TR29. The result is that the control pin of the square wave circuit, IC1 pin 11, is held high and +6.2 V is applied to IC6 via IC1 pins 13-14 and any of the switch sections of IC3 and IC4.

If all is well up to IC6 output, check IC8 output at IC8 pin 6. If D.C. is present here check IC8 and IC7. If not the fault is in the output stage(s).

The first output amplifier is a.c. coupled, and will not show d.c at the output due to faults on earlier stages, unless the offset voltage at IC8 output is negative, reverse biasing C13. If d.c. is measured at the output of amplifier TR15-TR28, but not at the first amplifier, the fault is in inverting amplifier TR15-28 or IC12.

The output d.c. offset is servoed to within ± 2 mV on each amplifier by low offset amplifiers IC11 and IC12. Measure the voltage at the outputs of IC11

and IC12 via a 1 k Ω resistor in series with the test lead (this prevents the capacitance of the meter causing the IC to oscillate). They should both be within ± 5 V. If not check IC11 or IC12 by replacement. If the fault persists check the voltages on the bases of the input transistor pairs, TR1 & TR2 or TR15 & TR16. There should be no more than 50 millivolts difference between them. If this is the case, check the other voltages around the discrete output amplifiers against those indicated on the circuit to locate the malfunction.

28.4.4 D.C On Output With Square Wave Selected Only

This can be due either to a fault causing the mark:space ratio of the square wave to be other than 1:1, or a voltage difference between the positive and negative half cycles of the square wave. Measure the d.c. voltage at the output of the voltage regulator IC19 (R57, R59 junction) with a D.V.M. This should be between +5.3 and 6.9 volts. Next measure the output of IC17 (pin 7). This should be a negative value within ± 20 mv of the voltage measured at IC19 output. If not, suspect IC17 or VR2 adjustment. Check the mark:space ratio by a dual trace oscilloscope, one trace connected to the output, and the other connected to the sine wave input at pin 37 of the edge connector. The side points of the square wave should correspond to the crossing points of the sine wave. If not check the d.c. content of the sine wave present at pin 37 with a D.V.M. If it is more than ± 20 mv, suspect a fault on the A1 board. If this is correct then suspect IC18.

28.4.5 Missing Output Level Values, Or Output Level Incorrect

Each detent in the continuous rotary level control produces a level change of 0.1 dB (5 dB per revolution). A level change of more than 0.1 dB/detent indicates a fault in one of the three level control stages, or associated latches. The list below indicates where to start looking:

less than 0.1 dB	suspect IC1, IC9, RN15 A & C
0.1- 0.7 dB	suspect IC5, RN8A, RN8B, RN9A
0.8- 5.6 dB	suspect IC7, RN10-14
6.4- 44.8 dB	suspect IC10, RN16-23

Always check the logic levels on the control inputs to the malfunctioning analogue switch ICs and associated resistors first. Rotate the level control and check each stage steps sequentially through the eight logic level combinations between minimum and maximum gain in each stage.

28.4.6 Symmetrical Clipping Above -21.2 dBu

If a high current (>1 A) flows in the output circuit, even briefly, relays RL3, RL4 and RL6 may become welded. A possible cause is plugging into a transformerless phantom-powered microphone input, which is capable of momentarily charging or discharging its input coupling capacitors through a very low resistance.

The MD404B, if so damaged, is only capable of delivering about ± 140 mV peak, and begins to square above this level. The ± 23 V supplies sometimes collapse (temporarily) due to the current limit in the power supply on the digital board.

28.5 A2 Card Calibration

28.5.1 Equipment Required

D.C. D.V.M. (3 1/2 digit).

MJS401D test set. It should have been calibrated recently (less than 6 months ago).

Extender card, PCB 76505.

28.5.2 Procedure

The board is factory calibrated, with the EPROM on the microcomputer board containing the requisite data to compensate for errors due to component tolerance variations. If "missing values" continue to be evident, despite following the fault finding procedures described earlier, return the entire oscillator to the factory for recalibration.

To adjust VR1 to VR3, follow the steps outlined below:

1/ Install MD404B on extender card in MJS401D main frame.

2/ Switch on power to MJS401D.

3/ VR3 is not fitted on later models, since it has a very small effect. If VR3 is fitted, it is sufficient to adjust it to halfway.

4/ Measure the voltage at IC19 output (centre pin). This should be in the region of 6.1 V. Adjust VR2 so that the voltage at IC17 output is exactly the same negative voltage as the positive voltage measured at IC19 output.

5/ MJS401D Front Panel Setup

Input	Load	Function	Filters	Rectifier	Scale	Dist'n	Coarse	Fine
--	Off	Read Osc	---	RMS	dB Exp	---	0	0

Set MD404B to 1 kHz, sine wave, and exactly 0 dBu out, using the fine level control.

Select square wave on MD404B. Adjust VR1 for exactly 0 dB output.

Select the sine wave output and check the MD404B output is still exactly 0 dB.

HIGHEST	MISSING
R70	
C62	
D10	
K20	
TR29	
VR3	

